AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions or listings of claims for this application.

Listing of Claims:

1. (Currently amended) A pixel sensor cell comprising:

a substrate;

a photoconversion device comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region;

a gate located over said photoconversion device;

a contact connected to said gate;

a charge collection region for receiving charges from said photoconversion device; and

a transistor for transferring charge from said photoconversion device to said charge collection region.

2. (Original) The pixel sensor cell according to claim 1 wherein said pixel sensor cell is arranged such that said photoconversion device has a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said contact.

3. (Original) The pixel sensor cell according to claim 2 wherein said gate reduces an energy barrier between said photoconversion device and said charge collection region.

4. (Original) The pixel sensor cell according to claim 1 wherein said gate comprises a dielectric substance layer and a polysilicon layer.

5. (Canceled).

6. (Currently amended) The pixel sensor cell according to claim 1 wherein said photoconversion device ~~includes~~comprises a pinned photodiode.

7. (Currently amended) The pixel sensor cell according to claim 1 wherein said charge collection region ~~includes~~comprises a floating diffusion region.

8. (Original) A pixel sensor cell comprising:

a substrate having a first surface level;

a photoconversion device having a first doped region of a first conductivity type and a second doped region of a second conductivity type located within said substrate;

a dielectric substance layer formed over the first surface level of said substrate thereby forming a second surface level;

a polysilicon layer formed over said second surface level;

a contact connected to said polysilicon layer; and

a transistor located adjacent to said photoconversion device.

9. (Original) The pixel sensor cell according to claim 8 wherein said dielectric substance layer has a thickness in the range of about 50-150 Å.

10. (Currently amended) The pixel sensor cell according to claim 8 wherein said dielectric substance layer ~~includes~~comprises silicon dioxide.

11. (Currently amended) The pixel sensor cell according to claim 8 wherein said dielectric substance layer ~~includes~~comprises silicon nitride (Si_3N_4).

12. (Currently amended) The pixel sensor cell according to claim 8 wherein said dielectric substance layer ~~includes~~comprises silicon oxynitride (SiON).

13. (Original) The pixel sensor cell according to claim 8 wherein said polysilicon layer has a thickness in the range of about 500-1500 Å.

14. (Currently amended) The pixel sensor cell according to claim 8 wherein said polysilicon layer ~~includes~~comprises silicon germanium.

15. (Currently amended) The pixel sensor cell according to claim 14 wherein said polysilicon layer ~~includes~~comprises silicon germanium in a ratio of about $Si_{60}Ge_{40}$.

16. (Currently amended) The pixel sensor cell according to claim 8 wherein said transistor ~~includes~~comprises a transfer transistor.

17. (Original) The pixel sensor cell according to claim 8 wherein said polysilicon layer overlaps at least a portion of said transistor.

18. (Original) The pixel sensor cell according to claim 8 wherein said pixel sensor cell is part of a CMOS imager.

19. (Original) The pixel sensor cell according to claim 8 wherein said pixel sensor cell is part of a charge coupled device (CCD) imager.

20. (Currently amended) An imager comprising:

an array of pixel sensor cells, each pixel sensor cell having a photoconversion device;

a substrate having a first surface level, said photoconversion devices being located within said substrate and comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region;

photodiode gates located over said substrate first surface level and over said photoconversion devices, and contacts connected to said photodiode gates; and

signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image.

21. (Original) The imager according to claim 20 wherein said photodiode gate further comprises a dielectric substance layer and a polysilicon layer.

22. (Original) The imager according to claim 20 wherein said imager is a CMOS imager.

23. (Original) The imager according to claim 20 wherein said imager is a charge coupled device (CCD) imager.

24. (Currently amended) A processing system comprising:

a processor; and

an imager coupled to said processor, said imager comprising:

a substrate having a first surface level;

a photoconversion device located within said substrate and comprising a region of a first conductivity type at a surface of the substrate and a region of a second conductivity type below the first conductivity type region;

a photodiode gate located over said substrate first surface level and over said photoconversion device, and a contact connected to said photodiode gate; and

a readout circuit comprising at least an output transistor formed on said substrate.

25. (Original) The system according to claim 24 wherein said photodiode gate further comprises a dielectric substance layer and a polysilicon layer.

26. (Original) The system according to claim 24 wherein said imager is a CMOS imager.

27. (Original) The system according to claim 24 wherein said imager is a charge coupled device (CCD) imager.

28. (Original) A method of forming a sensor, comprising:

forming a substrate having a first surface level;

forming a photoconversion device with a pinning voltage (V_{PIN}), said photoconversion device having a first doped region of a first conductivity type and a second doped region of a second conductivity type beneath said first surface level of said substrate;

forming a photodiode gate including a dielectric substance layer over said first surface level of said substrate, thereby forming a second surface level;

forming a polysilicon layer over said second surface level;

connecting a contact to said photodiode gate; and

forming a charge collection region for receiving charges from said photoconversion device.

29. (Original) The method according to claim 28 further comprising applying a negative bias to said contact, such that said photodiode gate acts to reduce said pinning voltage (V_{PIN}) of said photoconversion device.

30. (Original) The method according to claim 29 wherein said photodiode gate is arranged to reduce an energy barrier between said photoconversion device and said charge collection region.

31. (Original) The method according to claim 28 wherein said dielectric substance layer has a thickness in the range of about 50-150 Å.

32. (Currently amended) The method according to claim 28 wherein said dielectric substance ~~includes~~comprises silicon dioxide.

33. (Currently amended) The method according to claim 28 wherein said dielectric substance ~~includes~~comprises silicon nitride (Si_3N_4).

34. (Currently amended) The method according to claim 28 wherein said dielectric substance ~~includes~~comprises silicon oxynitride (SiON).

35. (Original) The method according to claim 28 wherein said polysilicon layer has a thickness in the range of about 500-1500 Å.

36. (Original) The method according to claim 28 wherein said polysilicon layer is formed of silicon germanium (SiGe).

37. (Original) The method according to claim 36 wherein said silicon germanium has a ratio of about $Si_{60}Ge_{40}$.

38. (Currently amended) The method according to claim 28 wherein said charge collection region ~~includes~~comprises a floating diffusion region.

39. (Original) The method according to claim 28 further comprising a transfer transistor.

40. (Original) The method according to claim 39 wherein said second polysilicon layer overlaps at least a portion of said transistor.

41. (Original) The method according to claim 28 wherein said sensor is part of a CMOS imager.

42. (Original) The method according to claim 28 wherein said sensor is part of a charge coupled device (CCD) imager.

43. (New) The imager according to claim 20 wherein said pixel sensor cells are arranged such that said photoconversion devices have a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said contacts.

44. (New) The imager according to claim 20 wherein said gates reduce an energy barrier between said photoconversion devices and said charge collection regions.

45. (New) The system according to claim 24 wherein said pixel sensor cell is arranged such that said photoconversion device has a reduced pinning voltage (V_{PIN}) when a negative bias is applied to said contact.

46. (New) The system according to claim 24 wherein said gate reduces an energy barrier between said photoconversion device and said charge collection region.